TRANSMITTAL FORM

Attorney Docket No. RPS920030107US1 2874P

In re the application of: **CRANFORD et al.**

Confirmation No: **4851**

Serial No: **10/685,022**

Group Art Unit: **2816**

Filed: **October 14, 2003**

Examiner: **Nguyen, Minh T.**

For: **Circuit and Method for Reducing Jitter in a PLL of High Speed Serial Links**

ENCLOSURES *(check all that apply)*					
☐	Amendment/Reply	☐	Assignment and Recordation Cover Sheet	☐	After Allowance Communication to Group
	☐ After Final	☐	Part B-Issue Fee Transmittal	☐	Notice of Appeal
☐	Information disclosure statement	☐	Letter to Draftsman	■	Appeal Brief
	☐ Form 1449	☐	Drawings	☐	Status Letter
	☐ (X) Copies of References	☐	Petition	■	Postcard
☐	Extension of Time Request *	☐	Fee Address Indication Form	☐	Other Enclosure(s) (*please identify below):*
☐	Express Abandonment	☐	Terminal Disclaimer		
☐	Certified Copy of Priority Doc	☐	Power of Attorney and Revocation of Prior Powers		
☐	Response to Incomplete Appln	☐	Change of Correspondence Address		
☐	Response to Missing Parts	*Extension of Term: Pursuant to 37 CFR 1.136, Applicant petitions the Commissioner to extend the time for response for xxxxxx month(s), from to .			
	☐ Executed Declaration by Inventor(s)				

CLAIMS					
FOR	Claims Remaining After Amendment	Highest # of Claims Previously Paid For	Extra Claims	RATE	FEE
Total Claims	20	23	0	$ 50.00	$ 0.00
Independent Claims	3	3	0	$200.00	$ 0.00
				Total Fees	$ 0.00

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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Attorney Name	Joseph A. Sawyer, Jr., Reg. No. 30,801
Signature	
Date	October 3, 2005

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Docket No: **RPS920030107US1** **2874P** Serial No: **10/685,022** Inventor(s): **CRANFORD et al.**	Date: **October 3, 2005** Filed: **10/14/2003**
Title: **Circuit and Method for Reducing Jitter in a PLL of High Speed Serial Links**	

- ■ Transmittal
- ■ Appeal Brief
- ☐ Executed Declaration
- ☐ Assignment + Recordation Sheet
- ☐ Information Disclosure Statement
- ☐ Form 1449 with ____ References
- ☐ Part B-Issue Fee Transmittal
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Saundra D. Hunter

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:

Hayden CRANFORD, Jr., et al.

Serial No: 10/685,022

Filed: October 14, 2003

Date: October 3, 2005

Confirmation No: 4851

Group Art Unit: 2816

Examiner: Nguyen, Minh T.

For: CIRCUIT AND METHOD FOR REDUCING JITTER IN A PLL OF HIGH SPEED SERIAL LINKS

APPEAL BRIEF

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TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

Appellant respectfully submits that International Business Machines Corporation is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

Appellant states that no such proceeding exists.

III. STATUS OF CLAIMS

Claims 2-8, 10-16, and 18-23 are pending and stand rejected. Accordingly, claims 2-8, 10-16, and 18-23 are on appeal and all applied rejections concerning those claims are herein being appealed.

IV. STATUS OF AMENDMENT

Application Serial No. 10/685,022 (the instant application) as originally filed included claims 1-23. Claims 2-8, 10-16, and 18-23 are pending. Claims 2-8, 10-16, and 18-23 are on appeal and all applied prospective rejections concerning claims 2-8, 10-16, and 18-23 are being appealed herein. All amendments made to the instant application have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention provides circuits and a method for reducing jitter in a high speed serial link.

Independent claim 2 recites a circuit comprising: a voltage controlled oscillator (VCO); a regulator coupled to the PLL to provide a supply voltage to the PLL; and a regulator control circuit coupled to the PLL and to the regulator for examining at least one parameter related to performance of the VCO, including a VCO control voltage, and for controlling adjustments of the supply voltage based on the examination.

Independent claim 10 recites a regulator control circuit comprising: decision logic for examining at least one parameter related to performance of a voltage controlled oscillator (VCO) in a phase-locked loop (PLL), including a VCO control voltage, comparator logic coupled to the decision logic for comparing the VCO control voltage to predetermined voltage levels, and controlling adjustments of a supply voltage to the VCO based on the examining.

Independent claim 18 recites a method comprising: examining at least one parameter related to performance of a voltage controlled oscillator (VCO) in the PLL, including a VCO control voltage, and the method also comprising controlling adjustment of a supply voltage to the VCO based on the examining.

Support for independent claims 2, 10, and 18 is found in the combination of Figure 2; page 3, lines 8-12; page 4, line 13, to page 5, line 16, and page 7, lines 1-5.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellant respectfully seeks review of the following rejections:

1. Claims 2-7, 10, 12-16, and 18-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishii.

2. Claims 8 and 11 are rejected under 35 U.S.C. 103(a) as obvious over Ishii in view of Chen.

VII. ARGUMENTS

A. Summary of the Applied Rejections

The Final Office Action dated May 25, 2005 rejected claims 2-7, 10, 12-16, and 18-23 under 35 U.S.C. 102(b) as being anticipated by Ishii, and claims 8 and 11 under 35 U.S.C. 103(a) as being obvious over Ishii in view of Chen. In making the rejection, the Examiner stated:

> **Claims 2-7, 10, 12-16 and 18-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishii, Japanese Application No. 122254/1999, printed on 3/10/2000. A copy of the US application No. 2003/0080817 is included in this Office action instead of the Japanese application No. 122254/1999.**
>
> **As per claim 2, Ishii discloses a circuit (Fig. 1) for reducing jitter (this limitation is merely the results when the circuit having the structure recited below operates) in a high speed serial link (this limitation is merely and intended use of the circuit), the circuit comprising:**
>
> **a phase-locked loop PLL (Fig. 1, see the title), the PLL comprising a VCO (VCO 6);**
>
> **a regulator (9) coupled to the PLL to provide a supply voltage (paragraph 30, lines 3-6, i.e., "sets a power supply voltage applied to the VCO 6") to the PLL; and**
>
> **a regulator control circuit (controller 8, see Fig. 3 for details) coupled to the PLL and to the regulator (as shown, these elements are connected) for examining at least one parameter related to performance of the VCO (paragraph 35, line 2, "various parameters, paragraph 36, lines 1-4, one of the parameter would be the oscillation frequency of the VCO), including a VCO control voltage (paragraph 45, i.e., the VCO control voltage does not greatly change even if the oscillation frequency changes. In other words, the VCO control voltage is monitored by the regulator control circuit 8, when the frequency of oscillation changes is detected, the regulator control circuit 8 changes the power supply voltage applied to the VCO to ensure the VCO control voltage to remain the same) and for controlling adjustments of the supply voltage based on the examination (paragraph 36, line 4)...**
>
> **Claims 8 and 11 under 35 U.S.C. 103(a) as obvious over Ishii, Japanese Application No. 122254/1999 in view of Chen (US Patent No. 5,463,352).**
>
> **As per claim 8, Ishii discloses a circuit (Fig. 1) having a regulator control circuit (Fig. 3) which includes a CPU 12 as discussed in claim 2 herein above wherein the CPU 12 performs functions which requires comparator logic, measurement logic and decision logic as explained in claim 10 above. Ishii does not explicitly disclose the reference voltages generated from a bandgap based reference generator as called for in the claim.**
>
> **Chen teaches a circuit for providing different supply voltages to a PLL as Ishii's reference. In column 2, lines 6-12, Chen explicitly teaches the needed reference voltages can be generated on chip using bandgap reference voltage source.**
>
> **It would have been obvious to a person skilled in the art at the time of the invention was made to generate the reference voltages for comparing in the Ishii's CPU 12 using on chip bandgap reference voltage source, i.e., incorporate a bandgap reference voltage source in the CPU 12. The motivation would be to reduce the number of components needed to implement the circuit...**

The Examiner stated the following in response to the previous arguments against these rejections:

> **Applicant's argument filed 3/14/05 has been fully considered but it is not persuasive.**
>
> **The argument is that Ishii fails to teach of suggest the VCO control voltage is monitored. In paragraph 45, Ishii merely teaches the VCO control voltage rarely changes.**
>
> **As understood by a person skilled in the art, the basic operation of a PLL is that the VCO control voltage is generated based on the phase difference between a reference clock and a feedback clock. The higher the VCO control voltage, the higher the frequency of the clock generated by the VCO. In the Ishii' reference, Ishii teaches that the VCO control voltage does not greatly change even if the oscillation frequency changes because the fact that the regulator control circuit 8 changes the voltage level of the power supply 9 which supplies the power for the VCO. In other words, in order to ensure the VCO control voltage remains constant when the oscillation frequency changes, the regulator control circuit 8 must have a means to directly or indirectly monitor the changes of the VCO control voltage. The act of "controlling adjustments of a supply voltage to the VCO based on the examining" is explicitly disclosed in paragraph 42, i.e., "By changing the power supply voltage of the VCO 6, ... the control voltage of the VCO 6 hardly changes, ..."**

The Examiner stated the following in the Advisory Action dated August 3, 2005:

> **Continuation of 11. does NOT place the application in condition for allowance because:**
>
> **The rejections of record are still believed to be proper, and therefore, are maintained. As admitted by the applicants, Ishii teaches a method and an apparatus for controlling the control voltage of the VCO (Remarks/Arguments, page 11, line 19) by adjusting the power supply voltage provided to the VCO (figure 1, the VCO power supply voltage setting device 9 powers the VCO). In other words, Ishii's apparatus must have a means to examine the control voltage of the VCO in order to be able to control the control voltage of the VCO because it makes no sense to control the VCO control voltage parameter without monitoring the parameter. The applicants' argument is not found persuasive because the argument fails to show that there is no need to examine the VCO control voltage in order to control the VCO control voltage in the Ishii's circuit as asserted by the examiner in the previous office action.**

Appellants respectfully request that the Board reverse the Examiner's final rejection of the pending claims.

B. The Cited Prior Art

Ishii discloses a PLL frequency synthesizer using a charge pump. In order to reduce the possibility of disturbing the drain/absorption balance of a charge pump in the PLL frequency synthesizer using the charge pump, when the output voltage and output current of the charge pump come close to their driving limits, the power supply voltage of a voltage-controlled oscillator is changed to cancel a change in input voltage of the voltage-controlled oscillator. The CPU in the controller calculates a VCO power supply voltage suitable for the frequency at the same time as it performs an oscillation frequency setting operation, and sends the result to the VCO power supply voltage setting device. A signal from an oscillation frequency setting frequency division number designating unit is sent to frequency division number setting registers in a reference divider and prescaler. The controller sends a control signal to the VCO power supply voltage setting device in accordance with a prospective frequency to be locked after switching. The VCO power supply voltage setting device adjusts the power supply voltage of the VCO in accordance with the signal. By changing the power supply voltage of the VCO, the bias of the oscillator in the internal circuit changes to change the oscillation frequency. Even if the control voltage of the VCO hardly changes, the frequency can be greatly changed. In other words, the control voltage of the VCO does not greatly change even if the oscillation frequency changes. This occurs because if a voltage from the VCO power supply voltage setting device is changed in synchronism with an output from the charge pump, two inputs cancel each other, and the control voltage of the VCO rarely changes. (Abstract, page 2, paragraphs 0036, 0041, 0042, and 0045).

Chen discloses a supply voltage tolerant phase-locked loop circuit that can operate at a

plurality of dissimilar supply voltages. By adjusting the frequency range of a PLL based on the power supply voltage, the same PLL design can operate at different supply voltages. (Abstract.)

C. Independent claims 2, 10, and 18 are allowable over Ishii

The present invention provides a method and circuit for reducing jitter in a phase locked loop (PLL) of a high-speed serial link. In accordance with the present invention, the method includes examining at least one parameter related to performance of a voltage controlled oscillator (VCO) in the PLL, including a VCO control voltage, and controlling adjustment of a supply voltage to the VCO based on the examinations. A regulator control circuit performs this examination and controls the resultant supply voltage to the PLL. Through the present invention, jitter in a PLL is successfully reduced by examination of the parameters directly related to PLL performance without knowledge of absolutes in frequency from the reference clock or in operating frequency. Thus, a flexible and efficient approach to accommodating variations in the frequency of the incoming signal for a PLL of a high-speed serial link is achieved. Ishii does not teach or suggest these features, as discussed below.

Ishii does not teach or suggest the "a regulator control circuit coupled to the PLL and to the regulator for examining at least one parameter related to performance of the VCO, including a VCO control voltage, and for controlling adjustments of the supply voltage based on the examination," as recited in independent claim 2. The Examiner has referred to the controller (element 8) of Ishii as being the same as the regulator control circuit of the present invention. The Examiner has stated that the control circuit of Ishii must have a means to monitor the changes of the VCO control voltage. However, the controller of Ishii is different from the regulator control circuit of the present invention, because the controller of Ishii does **not** examine the "VCO control voltage." In fact, the controller of Ishii does not appear to "examine" any parameter related to the performance of the VCO. Instead, Ishii teaches that the controller calculates the power supply voltage based in a "prospective frequency." Specifically, Ishii states:

> The CPU 12 in the controller 8 calculates a VCO power supply voltage **suitable for the frequency at the same time as oscillation frequency setting operation**, and sends the result to the VCO power supply voltage setting device 9. A signal from the oscillation frequency setting frequency division number designating unit 13 is sent to frequency division number setting registers (neither is shown) in the reference divider 2 and prescaler 7. (Page 2, paragraph 0036.)

> In this case, the controller 8 sends a control signal to the VCO power supply voltage setting device 9 **in accordance with a prospective frequency to be locked after switching**. The VCO power supply voltage setting device 9 adjusts the power supply voltage of the VCO 6 in accordance with the signal. (Page 2, paragraph 0041.)

Nowhere does Ishii mention a regulator control circuit that examines a "VCO control voltage" and that controls adjustments of the supply voltage "based on the examination" as in the present invention. In fact, referring to Figure 1 of Ishii, the flow of signals shown clearly illustrates that the controller sends a signal to the prescaler and to the VCO power supply voltage setting device. Nowhere does Figure 1 of Ishii show that the controller receives signals from the PLL. Clearly, the output voltage of the VCO is not sent back to the controller but is instead sent back to the phase comparator via the prescaler. Referring to Figure 3 of Ishii, instructions for the VCO power supply voltage setting device come from the CPU. This is further supported on page 2, paragraph 0035, of Ishii.

Furthermore, the Examiner has referred to paragraph 0042 of Ishii, apparently to show that the regulator control circuit of Ishii must have a means to monitor the changes of the VCO control voltage. However, paragraph 0042 of Ishii merely states that "even if the control voltage of the VCO 6 hardly changes, the frequency can be greatly changed." Specifically, Ishii states:

> By changing the power supply voltage of the VCO 6, the bias of the oscillator in the internal circuit changes to change the oscillation frequency. In other words, even if the control voltage of the VCO 6 hardly changes, the frequency can be greatly changed. (Page 2, paragraph 0042.)

In fact, Ishii describes in more detail how the control voltage of the VCO hardly changes. Ishii states:

> The gist of the present invention is that the control voltage of the VCO 6 does not greatly change even if the oscillation frequency changes. Therefore, **if a voltage from the VCO power supply voltage setting device 9 is changed in synchronism with an output from the charge pump 4, two inputs cancel each other, and the control voltage of the VCO 6 rarely changes**. (Page 3, paragraph 0045.)

Clearly, Ishii describes a method for controlling the control voltage of the VCO that teaches away from the present invention where controls adjustments of the supply voltage are based on the examination of the VCO control voltage.

Accordingly, Ishii does not teach or suggest the cooperation of elements as recited in the present invention. Therefore, claim 2 is allowable over Ishii.

Similar to independent claim 2, independent claims 10 and 18 recite, "examining at least one parameter related to performance of a voltage controlled oscillator (VCO)" in a PLL, and "controlling adjustments of a supply voltage to the VCO based on the examining." As described above, with respect to independent claim 2, Ishii does not teach or suggest these features. Accordingly, the above-articulated arguments related to independent claim 2 apply with equal force to claims 10 and 18. Therefore, claims 10 and 18 are allowable over Ishii for at least the same reasons as claim 2.

In view of the foregoing, Applicants respectfully submit that the recited invention is not taught, shown, or suggested by the cited art.

Dependent claims 3-7, 12-16, and 19-23 depend from independent claims 2, 10, and 18, respectively. Accordingly, the above-articulated arguments related to independent claims 2, 10, and 18 apply with equal force to claims 3-7, 12-16, and 19-23, which are thus allowable over the

cited references for at least the same reasons as claims 2, 10, and 18.

Accordingly, Appellant respectfully requests withdrawal of the rejection under 35 U.S.C. 102(b) and respectfully requests that the Board reverse the final rejection of claims.

D. Dependent claims 8 and 11 are allowable over Ishii in view of Chen

Dependent claims 8 and 11 depend from independent claims 2 and 10, respectively. Accordingly, the above-articulated arguments related to independent claims 2 and 10 apply with equal force to claims 8 and 11, which are thus allowable over the cited references for at least the same reasons as claims 2 and 10.

Furthermore, Applicants agree with the Examiner that Ishii does not explicitly disclose reference voltages generated from a band gap-based reference generator. To cure the defects of Ishii, the Examiner has relied on Chen and has referred to the column 2, lines 6-12, of Chen as teaching that reference voltages can be generated on chip using a bandgap reference voltage source.

However, Applicants respectfully submit that Chen does not teach the band gap-based reference generator, as recited in dependent claims 8 and 11. Referring to column 2, lines 6-12, of Chen, "a bandgap reference voltage source" is mentioned but nowhere does Chen show how to use the bandgap reference voltage source in the same way as the band gap-based reference generator of the present invention. Furthermore, Chen does not teach or suggest a band gap-based reference generator that is "coupled to comparator logic, the comparator logic coupled to measurement logic, and decision logic coupled to the measurement logic and to the comparator logic," as recited in dependent claim 8. Therefore, claim 8 is allowable over Ishii in view of Chen.

Similar to dependent claim 8, dependent claim 11 recites a "regulator control circuit" that includes a "band gap-based reference generator for establishing the predetermined voltage levels." As described above, with respect to dependent claim 8, Chen does not teach or suggest this feature. Accordingly, the above-articulated arguments related to dependent claim 8 apply with equal force to claim 11. Therefore, claim 11 is allowable over Ishii in view of Chen for at least the same reasons as claim 8.

In view of the foregoing, Applicants respectfully submit that the recited invention is not taught, shown, or suggested by the cited art.

Accordingly, Appellants respectfully request withdrawal of the rejection under 35 U.S.C. 102(b) and respectfully requests that the Board reverse the final rejection of claims.

E. Summary of Arguments

For all the foregoing reasons, it is respectfully submitted that claims 2-8, 10-16, and 18-23 (all the claims presently in the application) are patentable for defining subject matter, which would not have been unpatentable under 35 U.S.C. 102(b) and 35 U.S.C. 103(a) at the time the subject matter was invented. Thus, Appellants respectfully request that the Board reverse the rejection of all the appealed claims and find each of these claims allowable.

Note: For convenience of detachment without disturbing the integrity of the remainder of pages of this Appeal Brief, Appellants' APPENDICES A-C are attached on separate sheets following the signatory portion of this Appeal Brief.

Please charge any fee that may be necessary for the continued pendency of this application to Deposit Account No. 09-0460 (IBM Corporation).

Respectfully submitted,
SAWYER LAW GROUP LLP

October 3, 2005
Date

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APPENDIX A

CLAIMS

1. (Canceled)

2. (Previously presented) A circuit for reducing jitter in a high speed serial link, the circuit comprising:

a phase-locked loop (PLL), the PLL comprising a voltage controlled oscillator (VCO);

a regulator coupled to the PLL to provide a supply voltage to the PLL; and

a regulator control circuit coupled to the PLL and to the regulator for examining at least one parameter related to performance of the VCO, including a VCO control voltage, and for controlling adjustments of the supply voltage based on the examination.

3. (Original) The circuit of claim 2 wherein the regulator control circuit further determines if the VCO control voltage is within a predetermined range of optimum operation.

4. (Original) The circuit of claim 3 wherein the regulator control circuit further examines a lock status of the PLL.

5. (Original) The circuit of claim 4 wherein when the VCO control voltage is within the predetermined range and the PLL is locked, no adjusting of the supply voltage is done.

6. (Original) The circuit of claim 5 wherein when the VCO control voltage is not within the predetermined range or the PLL is not locked, the supply voltage is adjusted.

7. (Original) The circuit of claim 6 wherein the regulator control circuit further controls selection of a voltage level output from the regulator.

8. (Previously presented) The circuit of claim 2 wherein the regulator control circuit comprises a band gap-based reference generator coupled to comparator logic, the comparator logic coupled to measurement logic, and decision logic coupled to the measurement logic and to the comparator logic.

9. (Canceled)

10. (Previously presented) A regulator control circuit for reducing jitter in a high speed serial link, the circuit comprising:

decision logic for examining at least one parameter related to performance of a voltage controlled oscillator (VCO) in a phase-locked loop (PLL), including a VCO control voltage, comparator logic coupled to the decision logic for comparing the VCO control voltage to predetermined voltage levels, and controlling adjustments of a supply voltage to the VCO based on the examining.

11. (Previously presented) The regulator control circuit of claim 10 further comprising a band gap-based reference generator for establishing the predetermined voltage levels.

12. (Previously presented) The regulator control circuit of claim 10 further comprising measurement logic coupled to the comparator logic for measuring an output of the comparator logic against a predetermined range of optimum operation and providing an indicator signal to the decision logic.

13. (Previously presented) The regulator control circuit of claim 12 wherein the decision logic further examines a lock status of the PLL.

14. (Previously presented) The regulator control circuit of claim 13 wherein when the decision logic determines that the VCO control voltage is within the predetermined range based on the indicator signal and that the PLL is locked based on the lock status, no adjusting of the supply voltage is done.

15. (Previously presented) The regulator control circuit of claim 14 wherein when the decision logic determines that VCO control voltage is not within the predetermined range or the PLL is not locked, the supply voltage is adjusted.

16. (Previously presented) The regulator control circuit of claim 10 wherein the decision logic further controls selection of a voltage level output of a regulator supplying voltage to the VCO.

17. (Canceled)

18. (Previously presented) A method for reducing jitter in a phase-locked loop (PLL) of a high speed serial link, the method comprising:

(a) examining at least one parameter related to performance of a voltage controlled oscillator (VCO) in the PLL, including a VCO control voltage; and

(b) controlling adjustment of a supply voltage to the VCO based on the examining.

19. (Original) The method of claim 18 wherein the examining step (a) further comprises determining if the VCO control voltage is within a predetermined range of optimum operation.

20. (Original) The method of claim 19 wherein the examining step (a) further comprises examining a lock status of the PLL.

21. (Previously presented) The method of claim 20 wherein when the VCO control voltage is within the predetermined range and the PLL is locked, no adjusting of the supply voltage is done.

22. (Previously presented) The method of claim 21 wherein when the VCO control voltage is not within the predetermined range or the PLL is not locked, the supply voltage is adjusted.

23. (Original) The method of claim 18 wherein controlling step (b) further comprises controlling selection of a voltage level output of a regulator supplying voltage to the VCO.

APPENDIX B

EVIDENCE

(NONE)

APPENDIX C

RELATED PROCEEDINGS

(NONE)